2006 IEEE Jun-ichi Nishizawa Medal

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For pioneering contributions to dynamic random access memory (DRAM) cell structures and architecture

Hideo Sunami, Mitsumasa Koyanagi and Kiyoo Itoh

Hideo Sunami, Mitsumasa Koyanagi and Kiyoo Itoh are responsible for three of the major milestones in the evolution of modern dynamic random access memories (DRAMs). Their development of trench and stacked capacitor cells and the folded data line architecture resulted in unmatched high signal-to-noise ratio. Today, three decades after their invention, these cells and architecture remain the de facto standard for the DRAM industry.

Dr. Sunami was, in 1975, clearly ahead of his time when he invented the trench capacitor cell while the 4Kb DRAM was still the industry standard. This capacitor ultimately drove the development of dry etching, defect control and inspection associated with high-aspect ratio trenches. Today, the trench capacitor cell is used widely in commodity DRAM products and embedded applications. The concept also includes present cylindrical stack capacitor cells. He is currently a professor at the Research Center for Nanodevices and Systems, Hiroshima University in Hiroshima, Japan.

In 1976, Dr. Koyanagi devised the stacked capacity cell, the dominant DRAM cell since the 1-Mb generation came into being. His work has stimulated research and development on a variety of stacked capacitor cell structures, capacitor insulators and capacitor electrode structures, including those using hemispherical grain, high-k material and metal/insulator/metal. His work has also been applied to various memory devices having three-dimensional stacked structures. He is currently a professor in the Department of Bioengineering and Robotics, Tohoku University in Sendai, Japan.

In 1974, Dr. Itoh conceived the concept of the folded data-line architecture, which uses a pair of balanced data lines to eliminate various noise components. Since that time, this architecture has been adopted for nearly all DRAM chips since produced. A Fellow at Hitachi, Ltd. in Tokyo, where he is responsible for all research and development, he has also developed key DRAM devices and circuits such as the triple-well structure, on-chip voltage down-converters and subthreshold-current reduction circuits.

An IEEE Fellow, Dr. Sunami is the recipient of the IEEE Cledo Brunetti Award, the IEEE Electron Devices Society (EDS) Paul Rappaport Award and the Tokyo Governor's Award - Distinguished Inventor.

An IEEE Fellow, Dr. Koyanagi is the recipient of the IEEE Cledo Brunetti Award, SSDM Award of the International Conference on Solid-State Devices and Materials, Commendation by the Ministry of Education, Culture, Sports, Science and Technology - Person of science and technological merits (Japan), and the Okochi Memorial Technology Prize.

An IEEE Fellow, Dr. Itoh has received the IEEE Solid-State Circuits Award, the EDS Paul Rappaport Award, Commendation by the Minister of State for Science and Technology - Person of science and technological merits (Japan), the National Invention Award - Prize of the Patent Attorney's Association of Japan, and the national Medal of Honor with Purple Ribbon (Japan).