A CORRUGATED CAPACITOR CELL (CCC)

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***Abstract*—A new MOS dynamic random access memory (dRAM) cell named "CCC" has been successfully developed based on a one-device cell concept. This CCC is characterized by an etched-moat storage-capacitor extended into the substrate, resulting in almost independent increase in storage capacitance C_S of its cell size. A typical C_S value of 60 fF has been obtained with $3 \times 7\ \mu m^2$ CCC having a 4-μm deep moat and a capacitor insulator equivalent to 15 nm SiO_2 in thickness. The CCC is discussed in terms of its capacitance characteristics, dRAM operation with unit 32-Kbit array, some limiting factor to its closer packing, and future considerations.**

I. Introduction

SINCE THE first 1-Kbit dRAM [1] was introduced in the semiconductor market, four times greater integration has been achieved every three years in the past decade. This integration has maintained its advantage in higher density and lower cost over other types of memories. As a result, the present 64K dRAM has now reached maturity in production, and is being followed by the 256K dRAM development. This rapid evolution has been achieved mainly by the progresses in finer photolithography resulting in doubled packing density and circuit cleverness such as one-device cell [2] and address multiplexing. Although these progresses facilitate small cheap packaging, the chip size of the present 256K's approaches the maximum cavity size of the standard 16-pin dual-in-line package, as shown in Fig. 1. Therefore, forthcoming 1 Mbit dRAM will require an accelerated reduction of feature size leading to four times denser packing in order to maintain its great advantage over other memories.

Along with this greater integration, memory cells have also been reduced in size resulting in the decreases in capacitance area S and maximum storable charge, as shown in Fig. 2. However, storage capacitor value C_S has to be large enough to have sufficient S/N ratio [3] from the manufacturability and

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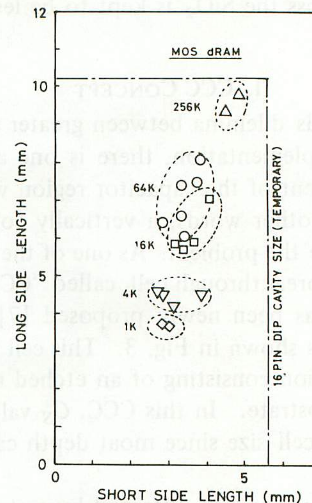

Fig. 1. Chip size increase in MOS dRAM's over commercially available chips provided by various manufacturers. About 1.4 times chip-size increase has been observed for four times greater integration of dRAM. Consequently, the chip size will soon meet a maximum cavity size of a 16-pin dual-in-line package.

the reliability standpoints. Regarding this S/N problem, a maximum storable charge Q_{ms} is preferred to be greater than 200 fC. In addition to the S/N problem, it is also better to be greater than 200 fC since an alpha particle [4] can produce hazardous electrons of greater than 200 fC at a typical maximum particle energy of 5 MeV. To supply large C_S value, the storage capacitor insulator has been decreasing in thickness with C_S area reduction.

However, this approach towards thinner insulator will soon meet its limit in the forthcoming 1-MBit dRAM in which chip size is kept below 50 mm^2 unless extremely tough and thin and/or high-permeability insulator is realized. An ordinary memory cell layout offers a C_S area of 5 to 10 μm^2. To provide 60 fF C_S, which facilitates highly stable dRAM operation [3], the SiO_2 must be thinner than 6 nm. Applying 5 V across the 6 nm SiO_2 causes almost 10 MV/cm electric field.

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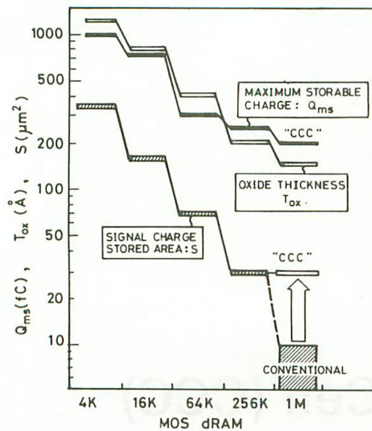

Fig. 2. Decreases in oxide thickness, storage capacitor area, and signal charge along with greater integration of dRAM's. Maximum storable charge Q_{ms} is defined as $C_S V_S$, where V_S is a signal voltage swing.

This immediately leads to catastrophic breakdown. Thus from the reliability and manufacturability standpoints, it is desirable that the field across the SiO_2 is kept to be less than about 2 MV/cm.

II. CCC Concept

To overcome this dilemma between greater integration and large C_S value implementation, there is one approach which provides enlargement of the capacitor region without increasing cell area. In other words, a vertically formed capacitor [5], [6] will solve the problem. As one of the vertical capacitor application, a breakthrough cell, called "CCC" (Corrugated Capacitor Cell), has been newly proposed [7]. A bird's eye view of the CCC is shown in Fig. 3. This cell is characterized by a capacitor region consisting of an etched moat which extends into the substrate. In this CCC, C_S value can increase independently of cell size since moat depth can increase also independently.

Storage capacitance values obtained by a static capacitance measurement are plotted in Fig. 4 for 4 × 8 and 3 × 7 μm^2 cell sizes. Almost linear increase in C_S value is obtained with increasing moat depth. If the moat stretches straightly into substrate, C_S is defined as $C_p + C_i L_{pm} d$, where C_p, C_i, L_{pm}, and d are capacitance of horizontal portion, insulator capacitance per unit area, perimeter length of horizontal shape of moat, and moat depth, respectively. Therefore, a gradient of the curve shown in Fig. 4 is $C_i L_{pm}$. A difference between two curves is caused by a difference in horizontal shape of moat, not in cell size. The 3 × 7 μm^2 cell has a rectangular-type horizontal moat pattern which measures 1.0 μm by 2.6 μm. As is shown in Fig. 4, C_S values for 3 × 7 μm^2 cells with and without a 4-μm deep moat are 60 and 8 fF, respectively, a 7.5 times C_S increase has been obtained. In other words, CCC can offer a very high storage capacitance with both small cell size and moderate insulator thickness.

III. Process and Capacitor Performance

A. Process Sequence

A fundamental process sequence to realize CCC structure is shown in Fig. 5. This is as follows:

Step-I. A triple layered insulator of CVD PSG/CVD Si_3N_4/thermal SiO_2 as an etching mask is provided to make deep moats into the Si substrate. Photoresist patterning of around 1 μm size is required for lithography.

Step-II. The Si substrate is etched with CCl_4 gas subsequent to an etching of the triple layer with $CF_4 + H_2$ gas. A moderate selectivity of around 8 is realized for Si to SiO_2 with CCl_4 gas. Slight wet etching of dry etched Si surface is subsequently added to remove slightly damaged and/or contaminated moat surface.

Step-III. A CVD Si_3N_4 film is deposited using LPCVD subsequent to thin bottom-oxide formation. A top layer of SiO_2 is also formed by thermal oxidation of Si_3N_4 resulting in extinction of possible pin holes and a protection film formation against dry etching of polysilicon plate which will be overlayed later on this capacitor insulator. Resultant triple layer of capacitor insulator is equivalent to 15 nm SiO_2 in thickness.

Step-IV. A first polysilicon deposition is performed to form polysilicon plate and is subsequently doped with phosphorus using $POCl_3$ gas. Then the second polysilicon is deposited on slightly oxidized first polysilicon surface. The second polysilicon deposition is used only to fill up remained moat. Then subsequent thermal oxidation makes intermediate insulator on the polysilicon plate. As a result, the wedge-shaped filled second-polysilicon is electrically floating, however, no harmful effect has not been found.

Thus these processes are easily applied to the conventional double polysilicon gate technology [8], [9] with high compatibility.

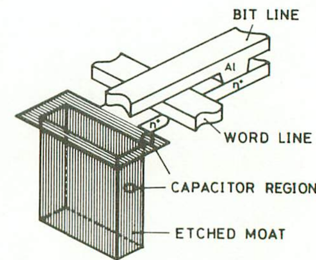

Fig. 3. Schematic cross section of a newly proposed dRAM cell named CCC (Corrugated Capacitor Cell) which is characterized by an etched moat as a storage capacitor.

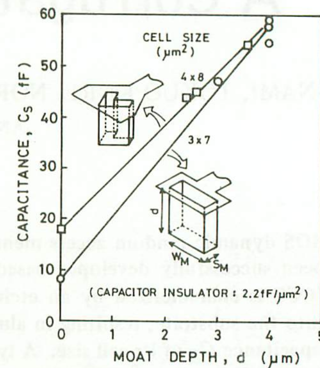

Fig. 4. Obtained storage capacitance increase for 4 × 8 and 3 × 7 μm^2 memory cells. A horizontal moat pattern measures 1.0 μm S_M by 2.6 μm W_M for 3 × 7 μm^2 cell. The capacitor insulator is a triple layer of $SiO_2/Si_3N_4/SiO_2$ of which thickness is equivalent to that of 15 nm SiO_2. Resultant capacitance per unit area is 2.2 fF/μm^2.

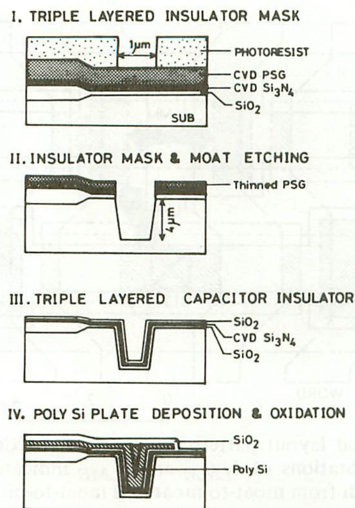

Fig. 5. Process sequence for CCC moat formation. This is easily added to the conventional double polysilicon gate processes.

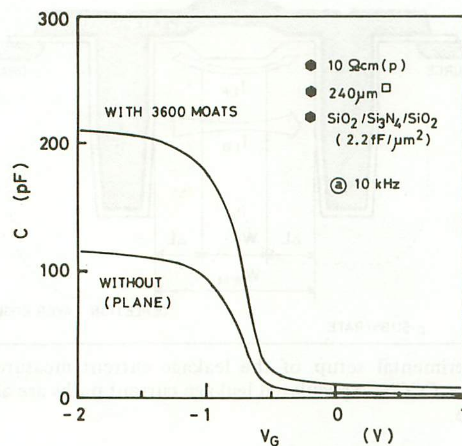

Fig. 6. Obtained C-V curves for nominal 240 $\mu m^{\square}$ capacitors with and without 3600 individual moats. Capacitor insulator is a triple layer of $SiO_2/Si_3N_4/SiO_2$ of which thickness is equivalent to that of 15 nm SiO_2. Resultant capacitance per unit area is 2.2 fF/μm^2.

B. Capacitor Performance

Capacitance-voltage (C-V) curves of capacitors with and without 3600 individual moats are shown in Fig. 6. There has been no significant difference with respect to interface state density and flat-band voltage V_{FB}. Furthermore, transient pulsed capacitance (C-t) and microwave minority-carrier-lifetime measurements have given no notable difference either. They have shown saturation time t_f of around 10 min and 80-150 μs, respectively, at room temperature. These values are on almost the same level with those in the conventional processes.

In this study, the triple layered capacitor insulator of $SiO_2/Si_3N_4/SiO_2$ is found far better than single oxide layer as far as infant mortality and short-term breakdown field strength are concerned. Breakdown voltage distributions are shown in Fig. 7 for the capacitors with and without 3600 moats. Slightly scattered distribution for cells with moats may originate not from moats themselves but from increased capacitor area since the breakdown voltage is defined as an applied gate voltage which induces 10 nA across the capacitor insulator for both capacitors in spite of the different area. An influence of keen

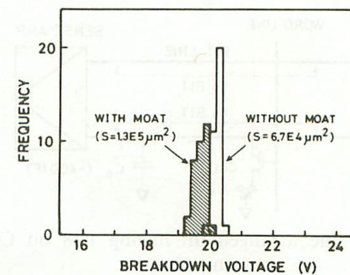

Fig. 7. Breakdown voltage distribution for nominal 240 $\mu m^{\square}$ capacitors with and without 3600 individual moats. Capacitor insulator is a triple layer of $SiO_2/Si_3N_4/SiO_2$ of which thickness equivalent to that of 15 nm SiO_2. Resultant capacitance per unit area is 2.2 fF/μm^2. S is an effective capacitance area.

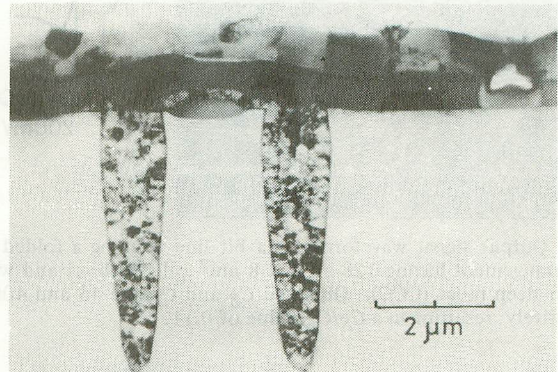

Fig. 8. A transmission electron micrograph of realized two CCC's having each 4-μm-deep moat. The moat is stuffed by double poly-Si deposition. Polysilicon grains are clearly shown in two moats.

edges of the moat on breakdown characteristics has not been found for the triple-layered insulator. On the other hand, 20-nm-thick single-oxide insulator results in breakdown voltages of 12 and 20 V for capacitors with and without 3600 moats, respectively. Keen edges obviously degrade the breakdown field strength of the single SiO_2 capacitor insulator. Further investigation will be made on long-term reliability for CCC capacitors.

A TEM cross section of realized two CCC's is shown in Fig. 8 Grains of polysilicon layer are clearly shown in the micrograph. The delineated moat shape is found to be sensitive to the dry etching environment. An optimum etching condition has realized the moat shape shown in Fig. 8.

IV. Memory Operation

A memory operation has been clarified with a unit array of 32Kbit. The array is composed of 256 folded-bit lines [10] having 128 bit of 4 × 8 μm^2 CCC with 2.5-μm deep moat, as shown in Fig. 9. The cell structure has already been shown in Fig. 3. To compare a difference in electrical performance of the cells accurately, two types of the cell with and without moat have been put into together in the same array. As C_S values for the cells with and without moat are 45 and 18 fF, respectively, a 2.5 times C_S increase has been obtained for the cell with moat in this sample. The same amount of C_S increase has been found also in dRAM's operation with identical CCC's. A storage capacitance C_S and a bit line capacitance C_D are 45 and 400 fF, respectively, resulting in C_S/C_D value of 0.11. Output signal waveforms are shown in Fig. 10 for the

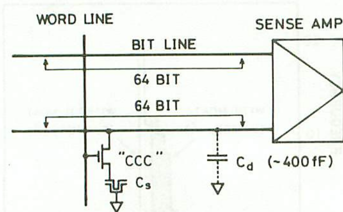

Fig. 9. Folded-bit line arrangement having 128 bit CCC's in 32-Kbit unit array.

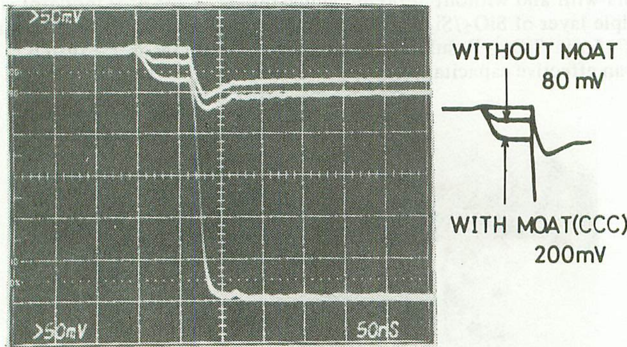

Fig. 10. Output signal waveforms of a bit line forming a folded data line arrangement having 128-bit 4 × 8 μm^2 cells without and with a 2.5-μm deep moat (CCC). Obtained C_S and C_D are 45 and 400 fF, respectively, resulting in a C_S/C_D value of 0.11.

cells with and without moat. A signal voltage of 200 mV has been realized with the CCC arrangement at 5-V power supply. An obtained S/N ratio is large enough to get very stable dRAM operation and high immunity to alpha particles for megabit dRAM's.

V. Limiting Factor Consideration

One of the biggest obstacle hindering closer packing of CCC's has been found to be a punchthrough current from one moat to the adjacent one, causing a loss of stored charge. An interference effect of adjacent cells are discussed in detail in terms of the leakage current between them.

A. Experimental Results

In an actual memory array, as shown in Fig. 11, some leakage currents have been observed. One is designated by I_{LMM} which flows through one moat to the adjacent one. The other is designated by I_{LMB} which flows through one moat to n$^+$-diffused layer connected to Al bit line.

As for dRAM operation, a leakage current of 10^{-13} A causes notable information loss of stored charges during one refresh cycle. A drain and/or plate voltage inducing 10^{-13} A is defined as V_{LTH}. (Leakage current itself will be shown later in Figs. 15 and 16.) A setup for the leakage current measurement is illustrated in Fig. 12. This V_{LTH} has been affected by moat to moat spacing W_{M-M} and moat to bit line (n$^+$-region) spacing W_{M-B} as shown in Fig. 13. In this paper, W_{M-M} and W_{M-B} are actual dimensions after devices are fabricated, but, a field oxide width W_F is a nominal one on photomask. Actual W_F is about 0.4 μm greater than the nominal one due to bird's beak.

In Fig. 13, it is clearly shown that the moat to moat leakage current I_{LMM} is dominant compared to I_{LMB}. The reason is

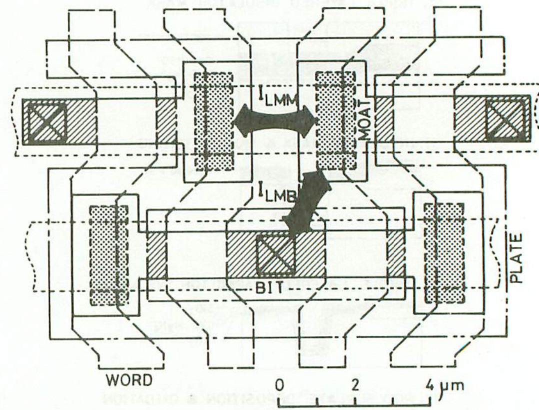

Fig. 11. A typical layout pattern for 3 × 7 μm^2 CCC array consisting of 4 cells. Notations of I_{LMM} and I_{LMB} indicate leakage currents flowing through from moat-to-moat and moat-to-bit line, respectively.

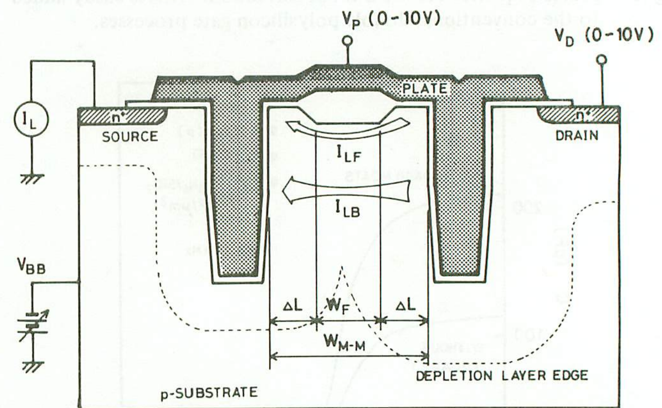

Fig. 12. Experimental setup of the leakage current measurement for two adjacent CCC's. Speculated leakage current paths are also shown in the figure.

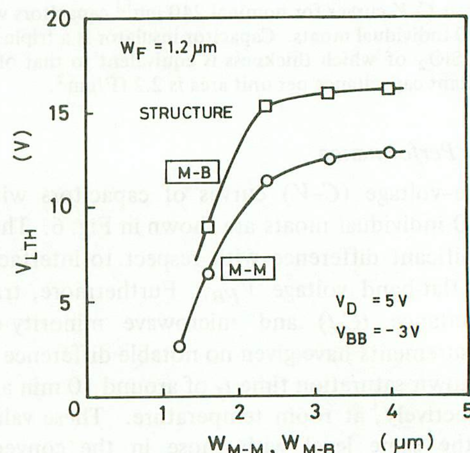

Fig. 13. Threshold voltage of leakage current V_{LTH} versus moat-to-moat spacing W_{M-M} for a pair of CCC's of which cross section is shown in Fig. 12. V_{LTH} is defined as a drain (bit line and/or plate) voltage which induces a leakage current of 10^{-13}A. The 10^{-13}A leakage current causes notable information loss of stored charges during one refresh cycle. Field oxide width W_F is an nominal one on photomask. Source and drain correspond to two adjacent bit lines.

speculated to be due to a punchthrough phenomenon in deeper portion of the substrate, as will be discussed later. Based on the experimental results, two leakage current paths are considered. One is a path for current, denoted by I_{LF}, which flows just underneath the field oxide, and the other, de-

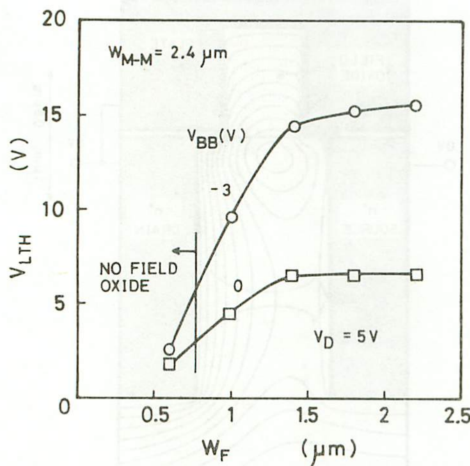

Fig. 14. Experimental results of V_{LTH} versus nominal field oxide width W_F for a pair of CCC's of which cross section is shown in Fig. 12.

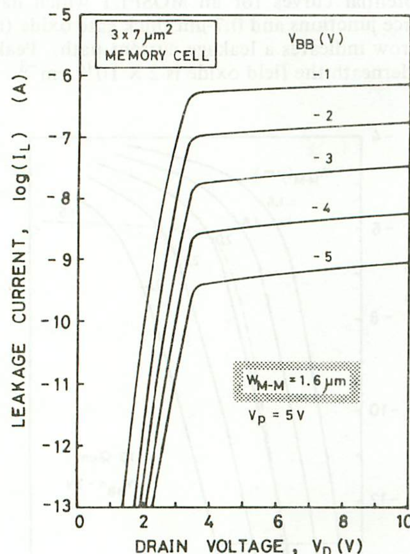

Fig. 15. Leakage currents between adjacent 3 × 7 μm^2 CCC's in memory array. Actual W_{M-M} is 1.6 μm and nominal W_F is 1.2 μm.

noted by I_{LB}, is a punchthrough current flowing through deeper portion of the substrate. As is shown in Fig. 14, a V_{LTH} becomes greater than 10 V at -3 V B_{BB} and this 10 V V_{LTH} is sufficiently high compared to 5-V operation. In addition, I_{LB} becomes dominant compared to I_{LF} in W_F region of greater than around 1 μm. No field oxide region has been formed in W_F region of less than 0.6 μm due to a practical resolution limit of 10 to 1 Reduction Projection Aligner. The reason why a V_{LTH} of around 2 V has been obtained for W_F below 0.6 μm is speculated to be due to boron field implant leakage. All of W_F values are 1.2 μm for CCC's discussed below, unless otherwise noted.

The leakage current has become appreciable for W_{M-M} of 1.6 μm, as shown in the next two figures, Figs. 15 and 16, for 3 × 7 μm^2 CCC of which layout has already been illustrated in Fig. 11. A moat width W_M is 2.6 μm unless otherwise noted. In these figures, there are two distinguishable leakage current regimes. One is steep line and the other is plateau region. These characteristics are very similar to a common-gate(plate) MOS transistor of which sources and drains are connected in

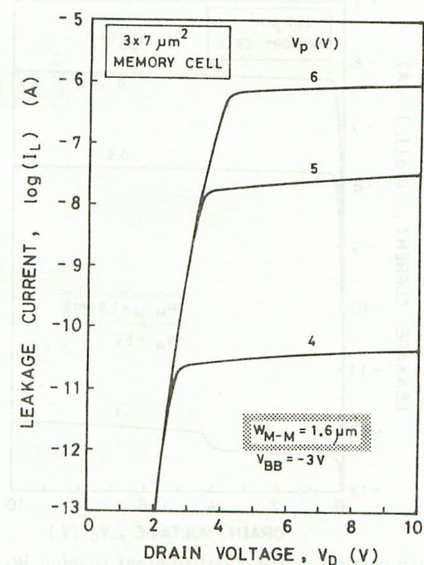

Fig. 16. Leakage currents between adjacent 3 × 7 μm^2 CCC's in memory array. Actual W_{M-M} is 1.6 μm and nominal W_F is 1.2 μm.

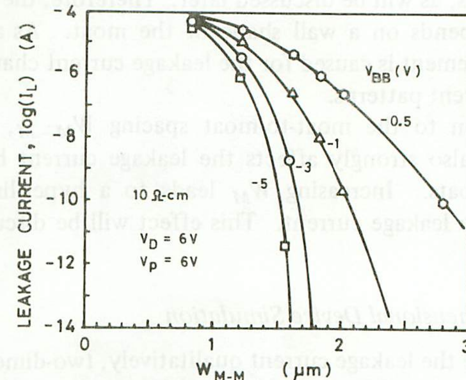

Fig. 17. Leakage current versus moat-to-moat spacing W_{M-M}.

series. Both side transistors have thin gate insulator(20-nm-thick triple-layered insulator) and relatively long channels along the moat wall. A center transistor has a thick gate insulator(around 500-nm-thick field oxide) and a high channel-dose(field channel stopper) and very deep source and drain simulated to two adjacent moats. Consequently, extremely strong dependence of the leakage current on moat-to-moat spacing is observed, as shown in Fig. 17. In case of 10 Ω · cm substrate, a W_{M-M} has to be greater than 1.8 μm at V_{BB} of -3 V.

As is expected in these considerations, leakage current for W_{M-M} of 1.8 μm has been found negligible at adequate conditions such as at 6 V V_{DD}, 6 V V_P, -3 V V_{BB}, and room temperature, as shown in Fig. 18. Some kink phenomenon is observed and is reproducible over various samples, however, this is not clarified yet. Therefore, the leakage current is of no importance to be taken into consideration when the moat to moat spacing W_{M-M} exceeds around 2 μm in case of 10 Ω · cm.

Regarding these leakage current characteristics cited above, slight disagreement has been found in different patterns as shown in Figs. 13 and 15. The reason is as follows: W_{M-M} is defined as the shortest distance between two adjacent moats. The leakage current, however, flows through a deeper portion

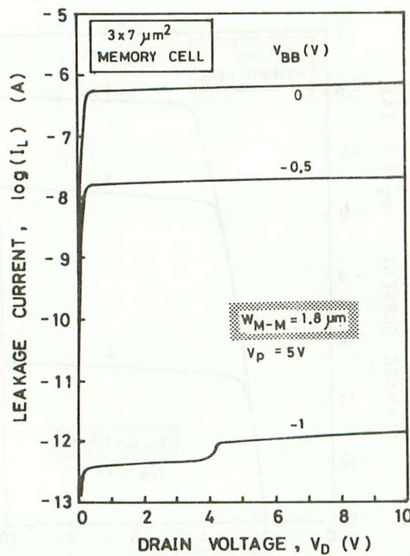

Fig. 18. Leakage current versus moat-to-moat spacing W_{M-M}. Actual W_{M-M} is 1.8 μm and nominal W_F is 1.2 μm. Leakage currents are far less than those of 1.6 μm shown in Fig. 15.

of the moats, as will be discussed later. Therefore, the current strongly depends on a wall shape of the moat. As a result, such disagreement is caused for the leakage current characteristics of different patterns.

In addition to the moat-to-moat spacing W_{M-M}, a moat width W_M also strongly affects the leakage current between adjacent moats. Increasing W_M leads to a hyper-linear increase in the leakage current. This effect will be discussed in Section VI.

B. Two-Dimensional Device Simulation

To outline the leakage current qualitatively, two-dimensional device simulation using CADDET [11] has been carried out. To simplify the analyses, a MOSFET has simulated actual CCC structure. A difference between the actual and the simulated characteristics has been found to be of considerable importance, as discussed later. However, the MOSFET which has deep source and drain and thick gate oxide (field oxide) has been used to simulate the actual structure, as shown in Fig. 19, because complicated device structures such as CCC, previously shown in Fig. 13, cannot be analyzed yet at present. The deep source represents a "low" level signal which means maximum electron charges are stored in the inversion layer. While, the deep drain denotes a "high" level signal which forms the deep depletion layer containing no electron charge.

Calculated drain current (leakage current) I_D versus drain voltage V_D curves are shown in Fig. 20. A broken line drawn also in the same figure is an experimental result for 1.6 μm W_{M-M}. There surely exists a significant difference. According to the simulation, a relation between W_{M-M} and impurity concentration of the substrate N_A with respect to various V_{LTH} is obtained as shown in Fig. 21. With increasing N_A, V_{LTH} also increases to some extent. Therefore, the use of lower resistivity substrate leads to reduced W_{M-M}, namely, denser packing of CCC's. In fact, the leakage current has been found negligible for a 4-Ω · cm substrate even with a W_{M-M} of 1.6 μm for which it has been appreciable for 10 Ω · cm, as

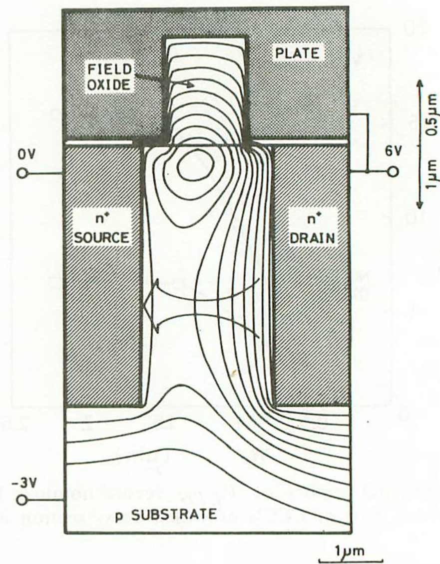

Fig. 19. Equipotential curves for an MOSFET which has 4-μm deep drain and source junctions and 0.7-μm thick gate oxide (field oxide in CCC). An arrow indicates a leakage current path. Peak boron concentration underneath the field oxide is 2×10^{16} cm^{-3}.

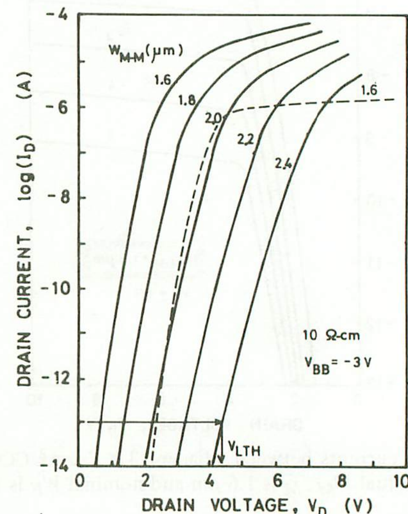

Fig. 20. Calculated leakage current characteristics for an MOSFET of which structure has already been illustrated in Fig. 19. A broken line is measured leakage current for 1.6 μm W_{M-M}.

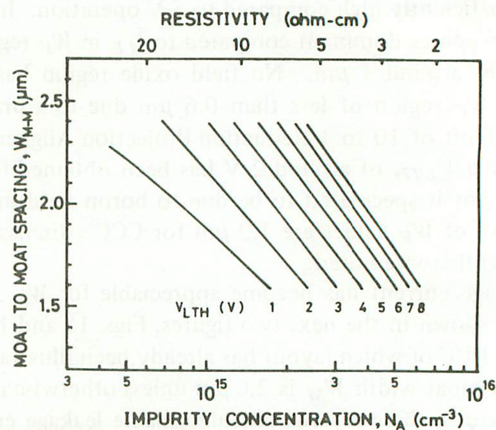

Fig. 21. Calculated V_{LTH} curves for moat-to-moat spacing W_{M-M} and impurity concentration N_A for CCC simulated MOSFET shown in Fig. 19.

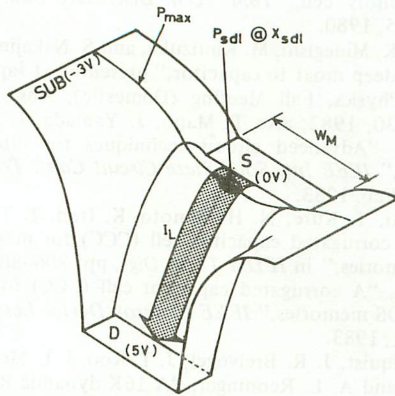

Fig. 22. Speculated three-dimensional potential distribution for a system of two moats (S: source and D: drain) and substrate. It is obvious that a saddle point potential is affected by a moat width W_M and V_{BB}.

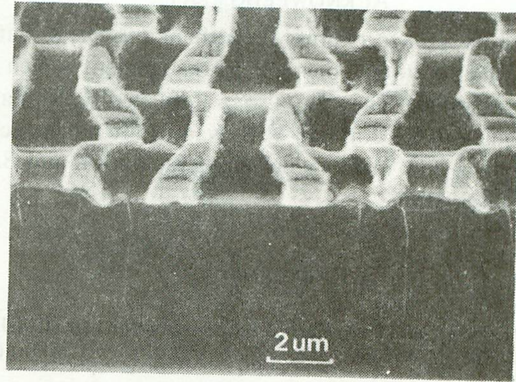

Fig. 23. SEM micrograph of horizontal plane and cross section of a portion of 32-Kbit unit array consisting of 3 × 7 μm^2 CCC's with 4-μm deep moats. This is at a step when word-lines are formed.

shown in Figs. 15 and 16. But it also causes some detrimental effects on circuit performances, such as increased back bias effect and increased parasitic junction capacitance.

VI. Discussion

Through the experimental investigation, the leakage current between adjacent moats has been found of considerable importance. Even if the simulation clarifies qualitative behavior of the leakage current, there still exists a poor coincidence between the simulation and the experimental results. For instance, it has been found that a V_{LTH} is less than 2 V at W_{M-M} of 1.8 μm for 10-$\Omega \cdot$ cm substrate. This value of 1.8 μm is significantly different from the experimental results shown in Figs. 17 and 18.

To explain the difference, it is thus speculated as follows. The simulation is, of course, two-dimensional numerical calculation which neglects an influence of bulk perpendicular to the cross section shown in Figs. 12 and 19. However, the potential distribution in the bulk along a direction perpendicular to the cross section has notable effect on the potential minimum where the leakage current flows.

Schematic view of the potential is shown in Fig. 22. If the potential minimum point is called "saddle" point X_{sdl}, a potential P_{sdl} at X_{sdl} has great influence on the leakage carrier (electron) which flows riding across the saddle point X_{sdl}, because the carrier density at X_{sdl} reveals Boltzmann's distribution and shows exponential like behavior. Therefore, when source and drain (moat) width W_M decreases, saddle potential P_{sdl} is raised by an influence of the substrate potential (V_{BB} of -3 V) resulting in exponential current decrease. These are present speculation to explain the poor coincidence between the simulation and the experimental results. In this sense, three-dimensional device simulation is needed to analyze the experimental quantitatively.

These behaviors of the leakage current discussed here imply constant current flow from one moat to the adjacent one. However, the leakage current in an actual dRAM operation is not constant since an amount of stored charges are limited. Then, a potential of one moat increases and that of the other decreases following to the charge transfer. This behavior is very similar to that of the charge-coupled device (CCD). Therefore, the leakage current analyses discussed in this paper can explain very early stage of the leakage current flow. Dynamic charge transfer behavior will be taken into future consideration.

VI. Conclusions

Based on the one-device cell concept a vertically structured dRAM cell named Corrugated Capacitor Cell (CCC) has been successfully developed. Since a storage capacitor is formed in an etched moat, almost linear increase in C_S value has been achieved with increasing moat depth. A typical C_S value of 60 fF has been obtained with 3 × 7 μm^2 cell having a 4-μm deep moat and a capacitor insulator equivalent to 15-nm SiO_2 in thickness. A C_S increase has also been clarified in 32 Kbit dRAM operation with a folded-bit line arrangement having 128 bit cells.

One of the biggest obstacles hindering closer packing of CCC's has been found to be a punchthrough current from one moat to the adjacent one, causing a loss of stored charge. As the results of experiments, it is found that moat-to-moat spacings of greater than 2 μm are large enough to suppress hazardous punchthrough current in case of 10-$\Omega \cdot$ cm substrate and 3 × 7 μm^2 memory cell.

Based on the experimental and analytical investigation of CCC, further integration of CCC is under development. A typical sample is shown in Fig. 23. This SEM micrograph shows a cross section of a memory array consisting of 3 × 7 μm^2 CCC's with 4-μm deep moats. An area layout of the array has already been shown in Fig. 11. A C_S value of 60 fF and a maximum storable charges of around 250 fC can be expected for this CCC array. This array has been successfully operated resulting in a signal of 250 mV.

This CCC will be very promising for forthcoming 1-Mbit dRAM and beyond because of its very large storage capacitance in small cell size with moderate insulator thickness from manufacturability and reliability standpoints. The future application of the CCC seems to be limited by the optical lithography, not by the device concept itself. On the basis of the CCC concept, further integration of denser packing has been under development.

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